UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,309	11/26/2003	Christian Pacha	V0195.0004	6833

38881 7590 06/22/2007

DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS 6TH AVENUE
NEW YORK, NY 10036-2714

EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

MAIL DATE	DELIVERY MODE
06/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,309	PACHA ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-32,34-37 and 39-52* is/are pending in the application.

4a) Of the above claim(s) *26 and 51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25,27-32,34-37,39-50,52 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the RCE filed 5/11/2007. Claims 25, 27-32, 34-37, 39-50 and 52-53 are under examination. Claim 26 has been withdrawn from consideration. Claim 51 is withdrawn from consideration for the reason as follow.

Election/Restrictions

Newly amended claim 51 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claim 51 reads on figure 7 that is a distinct species from the claims 25-37 and 39-50 read on generally on figure 3.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 51 has been withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 25, 27-31, 34-37, 45-50 and 52-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuzaki et al. (USP 6,500,715), prior art of record.

Figure 45 of Matsuzaki et al. shows a circuit arrangement comprising a flip flop (LH1 details shown in figure 8) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (MP1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CS/) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage(VSS) is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (TP1-TP3 within the INV1 whose details are shown in figures 8 and 14), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage), wherein each one of the terminals of the switching transistors (TP1 to TP3) has a defined electrical potential in the operating state (in the standby mode, the source, drain and gate terminals of the switching transistors have a defined electrical potential), a pulse generator circuit (NA1) that generates a flip flop input signal from an input signal (Ai, Aj) and from a clock signal (phi) and is coupled to the first power switch transistor and to the switching transistor as called for in claim 29.

Regarding claim 25, the flip flop (LH1) has two inverters.

Regarding claim 27, since the storage and the first power switching transistors have a higher threshold voltage, the thickness of the gate insulating layer of the storage transistors and

the first power switch transistor is greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claim 28, since the storage and the first power switching transistors have a higher threshold voltage, the channel width of the storage transistors and the first power switch transistor is less than the thickness of the gate insulating layer of the switching transistors.

Regarding claims 30 and 52, figure 14 shows a second power switch transistor (MP4, MN4) coupled to at least a portion of the switching transistors (TP1-TP3) such that in an operating state (standby mode) at least one supply voltage of the circuit arrangement is switched off, a gate terminal of each of the switching transistors coupled to the second power switch transistor has a predefined electrical potential (gate of TP1 to TP3 has a predefined potential Vdd).

Regarding claims 31-32 and 53, figure 14 shows a second power switch transistor (MP4, MN4) coupled to at least a portion of the switching transistors (TP1-TP3) such that in an operating state (standby mode) at least one supply voltage of the circuit arrangement is switched off, a source/drain terminal of each of the switching transistors coupled to the second power switch transistor has a predefined electrical potential (source of TP1 to TP3 has a predefined potential Vdd).

Regarding claims 34 and 37, figure 45 of shows the pulse generator (NA1) having transistors with low threshold voltages.

Regarding claims 35-36, figure 45 shows the subcircuit NA1 generates at least one flip flop input signal from at least one input signal Ai with a predetermined logic operation (nand logic operation).

Regarding claims 47-48, figure 45 of Matsuzaki et al. shows the protection transistors MP5, MN5 having high threshold voltage.

Regarding claims 45 and 50, figure 14 of Matsuzaki et al. shows the protection transistors MP4, MN4 having high threshold voltage.

Regarding claim 46, since the protection transistors have a higher threshold voltage, the thickness of the gate insulating layer of the protection are greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claim 49, in a first operating state, power switch MN1 switches off power supply to the switching transistors, the same control signal CS also electrically decouple the flip flop form the switching transistors, in a second operating state, the power switch MN1 connecting the power supply to the switching transistors, the protection circuit electrically couples the flip flop to the switching transistors.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. (USP 6,500,715) in view of Sani et al. (USP 6,794,914).

Figure 45 of Matsuzaki et al. shows a circuit arrangement comprising a flip flop (LH1 details shown in figure 8) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (MP1) having a second threshold

voltage (high threshold), wherein an application of a predetermined electrical potential (CS/) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage(VSS) is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (TP1-TP3 within the INV1 whose details are shown in figures 8 and 14), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage), wherein each one of the terminals of the switching transistors (TP1 to TP3) has a defined electrical potential in the operating state (in the standby mode, the source, drain and gate terminals of the switching transistors have a defined electrical potential), a pulse generator circuit (NA1) that generates a flip flop input signal from an input signal (Ai, Aj) and from a clock signal (phi) and is coupled to the first power switch transistor and to the switching transistor.

Matsuzaki et al. does not disclose a test circuit coupled to the flip flop for testing the functionality of the flip flop as called for in claim 39. Sani et al. shows a flip flop having a test circuit (310 of figure 3) to test and to enhance the reliability of the flip flop. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include Sani et al.'s test circuit in the circuit arrangement of Matsuzaki et al. for purpose of enhancing the reliability of the flip flop.

Regarding claim 40, the combination of Matsuzaki et al. and Sani et al. show the test circuit comprising a test input signal (Sin), output components (output of the flip flop) that reads a test output signal of the flip flop.

Regarding claim 41, the combination of Matsuzaki et al. and Sani et al. show the test circuit comprising a plurality of transistors (322, 324) having a high threshold voltage.

Regarding claim 42, since test transistors have a higher threshold voltage than the threshold voltage of the switching transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the switching transistors.

4. Claims 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. (USP 6,500,715) in view of Sani et al. (USP 6,794,914).

Figure 14 of Matsuzaki et al. shows a circuit arrangement comprising a flip flop (LH1 details shown in figure 8) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (MN1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CS) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage(VSS) is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (TP1-TP3), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage), wherein each one of the terminals of the

switching transistors (TP1 to TP3) has a defined electrical potential in the operating state (in the standby mode, the source, drain and gate terminals of the switching transistors have a defined electrical potential).

Matsuzaki et al. does not disclose test transistors, coupled to the flip flop, having a gate thickness greater than the gate thickness of the transistors of the pulse generator as called for in claims 43 and 44. Sani et al. shows a flip flop having a test circuit (310 of figure 3) to test and to enhance the reliability of the flip flop. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include Sani et al.'s test circuit in the circuit arrangement of Matsuzaki et al. for purpose of enhancing the reliability of the flip flop. Further, since test transistors have a higher threshold voltage than the threshold voltage of the pulse generator's transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the pulse generator's transistors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan T Lam
Primary Examiner
Art Unit 2816

6/16/2007